ABSTRACT OF THE DISCLOSURE

A low-jitter clock distribution circuit, used in an integrated circuit having multiple analog-to-digital converters (ADCs), includes a plurality of cascaded inverters, each inverter including an upper P-channel transistor connected to a lower N-channel transistor. The ratio Wp/Wn of the widths of the P-channel and N-channel transistors in each inverter is equal to substantially the square root of the ratio Un/Up of the majority carrier mobilities of the N-channel and P-channel transistors as determined by the semiconductor fabrication process.

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